Stage N° : 5

Contacts

Bernard DIENY,	bernard.dieny@cea.fr	Tel : 04.38.78.38.70
Lucian PREJBEANU	Lucian.prejbeanu@cea.fr	Tel: 04.38.78.91 43

Title

Magnetic tunnel junctions suitable for memory applications over a large range of operating temperatures

Keywords

Spin-electronics; Magnetic memory ; MRAM ; STT-MRAM ; magnetic tunnel junctions

Summary

There is an increase interest in microelectronics industry for a new type of magnetic non-volatile memory which have been developed in our lab for more than 10 years called STT-MRAM. In these memories, the storage elements are nanopatterned magnetic tunnel junctions which consist of two ferromagnetic layers separated by a thin tunnel oxide barrier (MgO). They are about to be introduced in products for consumer electronics. It is envisioned that they could play also a very important role in industrial and automotive applications but for the latter, the specifications are much more stringent in terms of reliability and operating temperatures (up to 150°C instead of 80°C for consumer electronics). In this internship and possibly the subsequent thesis project, we propose to explore several innovative routes in terms of materials and memory dot shape to reduce the influence of the operating temperature on the memory performances in particular in terms of retention (i.e. how long the information can be kept in the memory before being lost).

Details of subject

STT-MRAM are non-volatile memories based on magnetic tunnel junctions (MTJ). MTJ consist of two ferromagnetic layers separated by a very thin MgO tunnel barrier (1nm thick). The information is encoded in the magnetic orientation of one of the layer (called storage layer) while the magnetization of the other layer remains fixed. When a current flows through the junction, the resistance depends of the relative orientation of the magnetization of the two magnetic layers (Parallel=”0”=low resistance state; antiparallel=”1”=high resistance state). During write, the magnetic state of the storage layer is switched by a phenomenon called spin transfer torque which results from the exchange interaction between the spin of the tunneling electrons and those responsible for the magnetization of the storage layer. SPINTEC played a leading role in the development of magnetic memories based on these structures which are now about to be widely adopted by the microelectronic industry. This represents a major breakthrough which will significantly contribute to reducing the power consumption of electronic circuits. For some applications, further work is however still needed to increase the switching speed (to reach the ns regime with high reliability), to reduce the write current for downsize scalability and to increase the range of operating temperature. In this internship, we propose to investigate various approaches allowing to reduce the impact of temperature on the magnetic and electrical properties of the MTJ. Some of these approaches will rely on material optimization by using materials with high Curie temperature or with double MgO barriers and double polarizers. Another approach will rely on playing with the shape of the memory dot to exploit magnetostatic effects. Based on the previous experience of our laboratory, we propose to grow this type of stacks by sputtering, characterize their magnetic properties as well as their electrical properties at wafer level. We will then pattern the stacks in the form of nanometric pillars in our clean room and characterize their switching by spin transfer torque. The results will be benchmarked with the properties of the existing structures.

We hope that the internship will be pursued in a thesis. This would allow a thorough optimization of the stacks to reach specifications compatible with automotive and industrial applications

Requested skills
Basics in programming and magnetism

Possibility to follow with a PhD Yes