Proposal N° : **2**

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Title

Exploring the scalability of spintronics for 3D devices

Keywords
Magnetic random access memory, spintronics, semiconductor via, three-dimensional devices

Summary
Classical microelectronics is reaching its limits of downward scalability, reaching technological or scientific bottlenecks. Magnetic random access memories, based on magnetic tunnel junctions storing and reading bits of information, are emerging key ICT components. They are of immediate relevance for low-power and high-speed processor and mass-storage cache memory. Similar to other technologies, ways are being searched to design three-dimensional devices and thus allow long-term scalability in terms of areal density.
The scalability of single MRAM cells below 10nm lateral size has been demonstrated in the lab recently, independently at SPINTEC and at Tohoku university. The purpose of the internship is to pave the way towards integration of this concept in a viable technological process, compatible with high areal density and mass production. The principle relies on filling semiconductor vertical interconnects with a magnetic material, to be used as a storage cell. The first steps will consist in the structural, magnetic and electric characterization of such interconnects. At the scale of a PhD the work will be extended to fully functional memory cell, addressing both fundamental and technological challenges. This topic is a joint action between Spintec and LETI.

Full description of the subject

Technologies able to translate into the third dimension are expected to dominate over other technical solutions. This is the reason why flash memory, based on charge storage and reading, is the leading solution for USB and SSD storage, being able to stack tens of active layers. Nevertheless flash has limited endurance, rather high write power consumption and slow write rate. The emerging MRAM technology addresses these issues, however it is still a strictly 2D technology. The fabrication of MRAM with 3D features, starting from vertical-aspect ratio MRAM, suffers from limitations in etching technology.
Among the various technologies of non-volatile memories, STT-MRAM gathers a unique combination of assets: non-volatility, write speed (3-30ns), density (4Gbit demonstrated by Hynix/Toshiba), low consumption (a few tens of fJ/write), and very importantly an extremely long write endurance (>10^{13}cycles). Conventional STT-MRAM are based on out-of-plane magnetized magnetic tunnel junctions (MTJs) in which the storage layer magnetization is pulled out-of-plane thanks to a perpendicular anisotropy originating from the interface between the oxide barrier and the magnetic electrodes. In conventional STT-MRAM, this interfacial anisotropy is large enough to insure thermal stability of the storage layer magnetization down to diameter of the order of 20nm. To increase the STT-MRAM downsize scalability, a novel type of MRAM with much thicker storage was developed at SPINTEC. By drastically increasing the thickness of the storage layer to values comparable to its diameter, a perpendicular shape anisotropy (PSA) is induced in the storage layer which comes on top of the previously mentioned interfacial anisotropy with no penalty on the switching current. As a result, the perpendicular anisotropy is greatly reinforced enabling to maintain magnetic thermal stability (i.e. good memory retention) down to 4nm diameter. The name PSA-STT-MRAM was coined to designate this memory.

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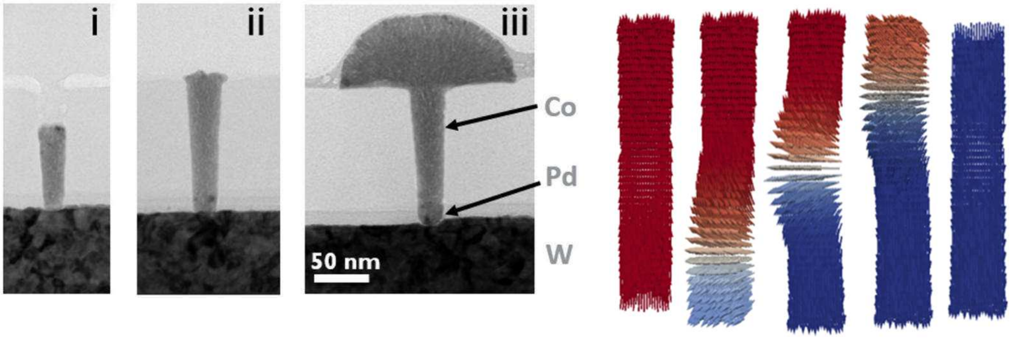

Illustration of vertical nanopillars (a) experiments and b) modeling.

Requested skills
nanosciences, nanotechnologies, solid state physics, basis of electronics

Possibility to follow with a PhD Yes