
Stage N° : 16

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Title

## Development of compact models for the design of hybrid CMOS/magnetic circuits based on newly discovered spintronics phenomena

Keywords
Spin electronics ; compact models ; CADENCE ; circuits design ; spin orbit

Summary
Spin electronics is a merging of microelectronics and magnetism which aims at taking advantage of the best of the two worlds. Magnetism is very appropriate for memory functions since it allows encoding information in a nonvolatile way via the direction of magnetization of magnetic nanostructures. Magnetic memories called MRAM (Magnetic Random Access Memories) are about to be launched in volume production at several major microelectronics companies. For readout, these memories use the tunnel magnetoresistance of magnetic tunnel junctions while the writing is performed by using the magnetic torque that a spin-polarized current exerts on the magnetization of a magnetic nanostructure (spin transfer torque). But spinelectronics keeps on progressing and new phenomena have been discovered since then on which our laboratory is actively working. These new phenomena which rely on spin-orbit interactions allow conceiving memories and non-volatile logic circuits exhibiting extremely low power consumption. The purpose of this internship will be to develop the compact models describing these new phenomena, integrate them within the CADENCE suite and design a few simple circuits based on these phenomena.

Details
SPINTEC is a laboratory entirely dedicated to spin-electronics and aiming at bridging basic research in magnetism with applications in microelectronics. Spin-electronics merge magnetism and microelectronics to try circumventing some of the limits of conventional CMOS microelectronics. In particular, a new type of non-volatile memories has emerged in the field called MRAM (Magnetic Random Access Memories). They combine a number of assets that no other type of memories gathers: non-volatility, speed, density and practically unlimited write endurance.
A number of academic studies have demonstrated the advantages that can be expected in terms of performances, energy consumption and new functionalities from the implementation of MRAM in electronic systems for various applications. Major industrial players are getting more and more interested by this technology, so far in its most standard version, i.e. based on spin transfer torque writing (STT). However, while the technology is getting more and more mature and close to commercialization, new generations are emerging, such as writing with voltage control of magnetic anisotropy and reading by conversion between spin current and charge current using spin-orbit effects. Even more interesting performances are expected from these new generations of circuits. However, those are still at the theoretical and material development levels.
Purpose of the internship :
The purpose of the internship will be to evaluate in a preliminary approach the advantages that could be obtained from memories and logic circuits based on these new phenomena, from electronics point of view. For that purpose, it will be necessary to develop compact models allowing to simulate electronic components based on these newly discovered phenomena, then to implement these models within CADENCE design suite. These design tools will

subsequently be used to design simple circuits and in the longer term evaluate more complex hybrid CMOS/magnetic circuits. Practically, two main tasks will be carried out during the internship:
-The development in VerilogA, of electric compact models for the simulation of electronic circuits based on these newly discovered phenomena;
-The design, based on these models, of read/write circuits for the emerging devices.
This internship will be continued by a PhD thesis aiming at a thorough evaluation of the performances of these components once implemented in more complex circuits, in particular the gain in terms of power consumption as well as new possible functionalities.

Requested skills
The candidate will have a Master 2, from University or Engineer School. His background will include analog microelectronic design, ideally using CADENCE software. Notions of programing with Verilog A would be a plus. The candidate will be fluent enough in spoken and written English for reading and writing articles in English. An interest for research and multidisciplinarity is required for this internship. A will to pursue with a PhD is strongly wished.

Possibility to follow with a PhD YES