Stage N° : 3

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Title:
Development of an ultra-fast SOT-MRAM

Keywords:
Magnetic memory, sub-ns pulses, nanofabrication, spin orbit interaction

Summary
The microelectronics industry will face major challenges related to power dissipation and energy consumption, and the microprocessors scaling will hit a power wall soon. A promising way to stop this trend is the integration of non-volatility in cache memories, the fastest memory located close to the processor. The development of an electrically addressable non-volatile memory combining high speed and high endurance is essential to achieve these goals.
The SOT-MRAM (Spin Orbit Torque MRAM), recently proposed by SPINTEC and developed by ANTAIOS, a start up company, (7 patent proposals), combines these features while being compatible with technological nodes below 22nm.
Its development is currently impeded by the necessity of a static in-plane applied magnetic field.
The purpose of this internship, and of the following thesis, is to develop a “field-free” SOT-MRAM.
This internship is experimental. It will be conducted under the supervision of both SPINTEC and ANTAIOS and will require nanofabrication in clean room, magnetic characterization and sub-ns magneto-transport measurements.

Details of subject
The microelectronics industry will face major challenges related to power dissipation and energy consumption, and the microprocessors scaling will hit a power wall soon. A promising way to stop this trend is the integration of non-volatility in cache memories, the fastest memory located close to the processor. Non-volatility (NV) of a memory means that it keeps the recorded information even if the power supply is turned off. The development of an electrically addressable non-volatile memory combining high speed and high endurance is essential to achieve these goals.
The SPINTEC laboratory has recently proposed a new magnetic memory concept, the SOT-MRAM for "Spin Orbit Torque MRAM", developed now by ANTAIOS (a start-up company from the laboratory). The SOT-MRAM is written by means of a current injected into a track supporting the magnetic nanopilar while the reading is done by measuring the tunnel magnetoresistance (TMR) by means of a current flowing through the stack perpendicularly to the layers (see figure). Compared to STT-MRAM (Spin Transfer Torque MRAM), which is being marketed very soon, notably by Samsung, and is about to become a memory standard, the SOT-MRAM, while being larger, has a much higher write speed (sub-ns) and an infinite endurance. These characteristics, plus its compatibility with technological nodes less than 22nm, make it the most promising candidate for SRAM replacement in cache memories.
Its development is currently impeded by the necessity of a static in-plane applied magnetic field during writing. Generating such a magnetic field poses integration problems and an integrated solution is indispensable to the development of these memories.
The role of this static magnetic field is to break a mirror symmetry. Without this break, the two opposite directions of the magnetization (coding "0" and "1") are perfectly equivalent and the information cannot be coded. This means

that possible solutions are not limited to the integration of a magnetic field but can be more diverse: pillar shape, particular material, particular writing scheme, etc.
The objective of the internship will be to focus on a particular solution that seems to Antaios and Spintec, the most promising in terms of scalability and distribution of critical parameters. Following the results of this internship, the thesis will continue on this solution or integrate other alternatives.
This experimental work will be carried out in the joint environment of SPINTEC and ANTAIOS, for the fundamental aspects (physics of spin orbit interactions, sub-ns magnetization reversal, ...) and applied one (most promising solution from industrial perspective, memory specifications , statistical tests, etc.). It will require nanofabrication in clean room, magnetic characterization as well as magneto-electrical transport under sub-ns pulses.

Requested skills
Master 2 solid state physics / Condensed matter physics / Material science

Possibility to follow with a PhD Yes/No
Yes

Figure

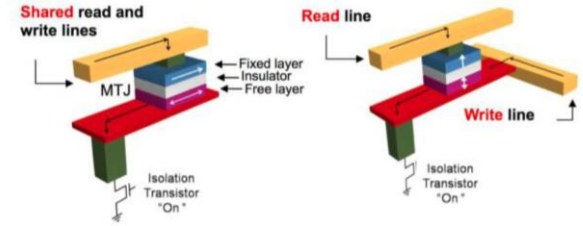

Figure 1: *In STT-MRAM (left), the read and write current share the same path while they are different for the SOT-MRAM (right).*