Proposal N° : 1

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Title
Magnetic memory optimized for ultra-low power consumption

Keywords
spintronic, magnetic memories, MRAM, ultra-low power consumption, quantum engineering

Summary
The power consumption of electronic circuits keep on increasing with their performances. This consumption has a static part associated with the leakage of the CMOS transistors and a dynamic part due to the charge/discharge of the interconnects during data transfer between memory and logic. In this context, magnetic memory can play an important role to save energy. These memories have been studied at SPINTEC for more than 10 years. They use spintronic phenomena (tunnel magnetoresistance, spin transfer torque, spin orbit torque...). They gather several assets: non volatility (ability to keep the information without being powered), speed (write/read in a few nanoseconds), density, write endurance. In a memory, there is always a tradeoff to find between the stability of the written information (memory retention) and the energy required to write. The research goal of the internship and of the PhD thesis which will follow, will be to optimize the magnetic tunnel junctions which constitute the memory dots (composition, shape, write process) to optimize this tradeoff with the aim of minimizing the power consumption depending on the required specifications for various types of applications (Smartphones, high power computing, quantum engineering...).

Full description of the subject
The subject proposed concerns spin electronics, a rapidly developing discipline combining electronics and magnetism. It is an extremely dynamic field of magnetism combining basic research and applications. Spin electronics has made a great contribution to the hard disk industry (read heads using giant magnetoresistance phenomena or tunneling) and is about to revolutionize microelectronics by introducing a new type of magnetic memory: MRAMs (Magnetic Random Access Memory). The memory cell consists of magnetic tunnel junctions (MTJ) whose core is formed of two magnetic layers (fixed magnetization reference layer and switchable magnetization storage layer) separated by a thin insulating barrier. The electrical resistance of these structures depends on the relative orientation (parallel or antiparallel) of the magnetizations of the two magnetic layers (tunnel magnetoresistance). These junctions are written in parallel or antiparallel magnetic configuration by current pulses crossing the junction using the spin transfer phenomenon. Their magnetic state is read again by measuring their electrical resistance. SPINTEC has played a very important role at the international level in the development of these memories which are about to return to volume production in the microelectronics industry. The first industrial application targeted is the replacement of embedded FLASH memories. But we always try to improve the properties, especially in terms of power consumption, writing speed, size of the memory points etc. to open other application fields (eg SRAM fast memories). The proposed subject aims to reduce their write power consumption by optimizing the composition, the shape of the memory points and by using recently discovered phenomena such as spin torque orbit or voltage control of magnetic anisotropy.

The proposal will combine modeling and experiments. This optimization requires an accurate evaluation of the barrier height separating the two states of the memory that must be introduced to ensure the specified retention time at the operating temperature. Then the composition of the tunnel junction, the size of the memory point and possibly its shape should be adjusted so that the magnetization of the storage layer remains stable against thermal fluctuations for the specified duration but without oversizing. To further minimize the consumption, low Gilbert damping materials are selected and spin transfer writing is combined with spin torque writing orbit and magnetic anisotropy lowering by the voltage applied across the junction.

The physics involved is well understood so that the modeling of these structures by simulation will be straightforward. The experiments will consist of depositing magnetic multilayers, nanostructuring (lithography, etching) in a clean room and then characterizing their magnetic and electrical properties.

Requested skills

nanosciences, nanotechnologies, solid state physics, basis of electronics

Possibility to follow with a PhD Yes