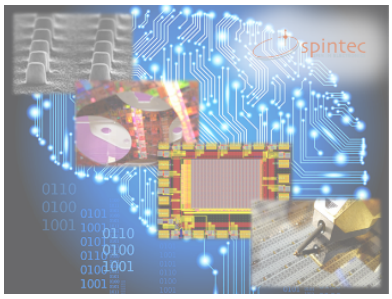
Recruitment of an Associate Professor permanent position on *digital and mixed signal design of emerging circuits and architectures*



SPINTEC

Positioned at the crossroad of science and technology, **SPINTEC** (**SPINtronique et TEchnologie des Composants**, http://www.spintec.fr) is one of the leading spintronics research laboratories worldwide. SPINTEC was created in 2002 and rapidly expanded to currently exceed 100 persons, of which 48 permanent staff from CEA, CNRS and Grenoble-Alpes University. The lab aims at bridging the gap between fundamental research and applications in spin electronics. As such, the outcome of the laboratory is not only scientific publications and communications at international conferences, but also a consistent patent portfolio and implementation of relevant functional demonstrators and device nanofabrication. The lab has launched four start-up companies in the past 12 years. This synergy has placed SPINTEC at the forefront of spintronics research, having actively contributed to the emergence in industry of spintronic memories called MRAM, on which the laboratory holds key patents.

SPINTEC benefits from an idea local environment with a large spectrum of opportunities:

- SPINTEC belongs with the Interdisciplinary Research Institute of Grenoble (IRIG), gathering 10 laboratories with of total of 1000 researchers, technicians, doctoral and post-doctoral students. IRIG covers interdisciplinary skills (physics, chemistry, biology), and provides access to cutting-edge scientific and technological platforms such as PTA cleanroom, and nano-characterization PFNC.
- The Giant Campus Site (also called Scientific Presqu'Ile) offers an exceptional scientific environment with partners such as CEA-LETI, Néel Institute and major European facilities (ESRF and ILL on the EPN Campus).
- The entire Campus of Grenoble Alpes University, whose excellence was recently recognized by the national IDEX award, bears a collective dynamics of research challenges in all fields of knowledge.

Grenoble is a cosmopolitan city at the heart of the French Alps. One out of five people living there works in the field of research, innovation or higher education. In addition, Grenoble offers various cultural and sportive opportunities all year round.

CONTEXT

Context. The last decade has seen the emergence of numerous studies around integrated nanoelectronic technologies for a growing number of application areas, ranging from the Internet of Things, to integrated components specialized in the management and optimization of energy consumption, environmental monitoring, safety and security in the automotive and space industries, support and control in the healthcare field, and hardware implementations of AI algorithms. Today's mature and emerging nanoelectronics technologies present a lot of challenges for the design and validation of digital and mixed-signal circuits and architectures. To enable these technologies to be used on a large scale, but in a rational way, breakthrough innovations are required to find the best tradeoff between computing power and power consumption. For instance, one of the key points is to rethink computing architectures, to overcome the limitations inherent to the classic Von-Neumann computing model. The general idea is to bring computation closer to the data to be processed, by moving it into memory peripherals (Near-Memory Computing), or even integrating it directly into the memory (In-Memory Computing). Another key point is the optimized design of digital computing core architectures based on emerging technologies, secure and safe in operation.

Context at SPINTEC. SPINTEC has major strengths in the development of these new paradigms, combining in a common momentum a large part of the required expertise: nanofabrication, electrical testing, theoretical

understanding and modeling of the physical and electrical involved phenomena, circuit and architectures design up to their integration in demonstrators. This has led to the laboratory's involvement in a number of major projects: a specific chair at the Grenoble-based MIAI artificial intelligence institute, international ANR-DFG NEUSPIN and ANR-NSF STOCHASPIN projects, and participation as a key partner in the PEPR Electronics, SPIN and IA - Emergence projects, started in 2023.

POSITION

Research. The hired person will join the "spintronics IC design" team, bringing complementary expertise in circuit design and architecture. The aim is to create a holistic chain of design and validation skills, covering all levels of abstraction and enabling the implementation of robust design/validation approaches, from circuit level to architecture and system level (models, physical and statistical exploration tools, fast design/synthesis and simulation of circuits and architectures, etc.). The position will also interface with other teams in the laboratory, in particular Artificial Intelligence and MRAM. His/her contribution will give new impetus and diversify the numerous collaborations with laboratories at national (LIRMM, INL, IM2NP, CNRS-Thales, EMSE, C2N, etc.) and international level (KIT, Univ. of Maryland, Univ Purdue, TU Dresden, Univ. Newcastle, IHP Microelectronics) as well as industrial partners (TowerJazz, TRAD, Greenwaves, ST Microelectronics, Tiempo IC, Dolphin, Idemia, Electronic Marin...).In-memory computing will occupy a privileged place, both for its importance in current developments in computing architectures, and for its relevance to emerging technologies such as spintronics (and MRAM), RRAM, PCM, etc. Whatever the design level considered, the inherent variabilities of these emerging technologies will have to be specifically taken into account. The ultimate aim will be to be able not only to design the elementary building blocks of these architectures (hardware gas pedals) systematically, but also to bring them up through the design flow so as to integrate them into a complete computing system.

Teaching. The candidate will teach in Phelma engineering school of Grenoble Institute of Technology, Grenoble INP. While reaffirming its three main pillars of physics, electronics and materials, Phelma is ensuring that the training of its engineering students and masters students evolves in line with the changing needs of the industry, linked primarily to energy and digital transitions. Embedded microelectronics and electronics account for around 25% of scientific teaching at Phelma, from transistors to embedded systems, including logic circuits, computer architectures, memories and embedded computing. The candidate will be involved in teaching VLSI digital microelectronics on ASIC and FPGA targets, hardware modeling languages (SystemVerilog, VHDL, etc.), design flow at system and circuit levels, design of optimized, energy-efficient circuits and architectures for embedded systems. He/she will also be involved in first-year analog electronics courses (conventional and apprenticeship), and in the Integrated Electronic Systems (SEI), Embedded Systems and Connected Objects (SEOC), Signal Images Communication and Multimedia (SICOM, joint course with Ense3) and Microelectronics Telecoms (MT) apprenticeship courses. As practical teaching plays an important role at Phelma, the candidate will be expected to provide a significant proportion of teaching in the context of design offices, projects and practical work.

Profile. The candidate should have research experience in several of the following fields: design and validation of digital or mixed circuits and architectures, hardware design for power and consumption optimization, design of reconfigurable, robust and secure systems-on-chip. His/her profile will mainly cover the highest levels of abstraction in microelectronics, from the implementation of the design flow and validation of architectures and systems, or in the design of integrated circuits at full custom level. The ability to teach in English is imperative, as a number of the school's courses are taught strictly in English. International experience is a definite asset.

How to apply: this position is likely to be published in the 2024 Associate Professor national recruitment campaign, to be announced in February 2024.

Potential candidates should contact: direction.spintec@cea.fr, attaching a complete CV, a cover letter and recommendation letters.