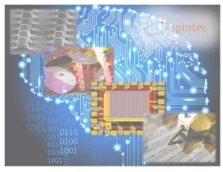

POST DOC Recruitment

FPGA-based and ASIC-based system level processor architecture development

SPINTEC Laboratory

Positioned at the crossroad of science and technology, SPINTEC (SPINtronique et TEchnologie des Composants, http://www.spintec.fr) is one of the leading spintronics research laboratories worldwide. SPINTEC was created in 2002 and rapidly expanded to currently exceed 110 persons, of which 50 permanent staff from CEA, CNRS and Grenoble-Alpes University. The lab aims at bridging the gap between fundamental research and applications in spin electronics. As such, the outcome of the laboratory is not only scientific publications and communications at international conferences, but also a consistent patent portfolio and implementation of relevant functional demonstrators and device nanofabrication. The lab has launched four start-up companies in the past 13 years. This synergy has placed SPINTEC at the forefront of spintronics research, having actively contributed to the emergence in industry of spintronic memories called MRAM, on which the laboratory holds key patents.

SPINTEC benefits from an ideal local environment with a large spectrum of opportunities:

- SPINTEC belongs to the Interdisciplinary Research Institute of Grenoble (IRIG), gathering 10 laboratories with a total of 1000 researchers, technicians, doctoral and post-doctoral students. IRIG covers interdisciplinary skills (physics, chemistry, biology), and provides access to cutting-edge scientific and technological platforms such as the PTA cleanroom and the nano-characterization platform PFNC.
- The Giant Campus Site offers an exceptional scientific environment with partners such as CEA-LETI, Néel Institute and major European facilities (ESRF and ILL on the EPN Campus).
- The entire Campus of Grenoble Alpes University, whose excellence was recently recognized by the national IDEX award, bears a collective dynamics of research challenges in all fields of knowledge.

Grenoble is a cosmopolitan city at the heart of the French Alps. One out of five people living there works in the field of research, innovation or higher education. In addition, Grenoble offers various cultural and sportive opportunities all year round.

CONTEXT AND MOTIVATIONS

Context. The last decade has seen the emergence of numerous studies around integrated nanoelectronic technologies for a growing number of application areas, ranging from the Internet of Things, to integrated components specialized in the management and optimization of energy consumption, environmental monitoring, safety and security in the automotive and space industries, support and control in the healthcare field, and hardware implementations of Artificial Intelligence (AI) algorithms. Today's mature and emerging nanoelectronic technologies present a lot of challenges for the design, validation and test of digital and mixed-signal circuits and architectures. An important aspect of such innovative technologies is their robustness against attacks, either laser or side-channel attacks, in particular processors for which the integrity has to be reinforced. Specific studies are mandatory for the most emerging technologies, which is the core of this project. The project aims to develop a RISC-V architecture with NV MRAM memory elements while ensuring compliance with security requirements. It will address 3 challenges: 1) the characterization of vulnerabilities of backup/restore mechanisms in NV processor, 2) the modeling of an innovative Voltage Gated Spin Orbit Torque (VG-SOT) MRAM cell as elementary cell to build blocks as register and memory and 3) the design of countermeasures from these blocks to mitigate hardware attacks. To reach these objectives, we will go through the evaluation of security advances taking profit of MRAM blocks and mitigation mechanisms as protection schemes at cell level, hardware level and software level. This project endeavors to pioneer a secure, non-volatile computing paradigm through innovative MRAM integration, addressing critical vulnerabilities and advancing protection mechanisms, thereby setting a new standard for secure edge computing architectures.

OBJECTIVES

The goal of the post-doctoral position is hence to

i) develop an FPGA test platform embedding MRAM memories from the market with the aim of validating a complete high level processor architecture
ii) participate to the development of a secured processor architecture in the framework of fault attacks
iii) develop an MRAM memory model based on last Magnetic Tunnel Junction generations.

The work environment is twofold, first FPGA-based for the first part and ASIC-based for the second part, both being at digital level. However, modeling a memory still requires to perform electrical simulations and characterizations. Thus, a multidisciplinary work is expected.

Keywords:

Memories, MRAM, FPGA platform, Characterization models, Integrated Circuit security

POSITION

Starting date / duration / location:

Post doctoral contract: October - November 2025 / 18-24 months / SPINTEC Laboratory Grenoble, France

REQUIRED SKILLS

The applicant must have a PhD degree in Microelectronics and/or Nanoelectronics, with skills in the fields of digital circuit design, and good knowledge of programming languages (Python, Matlab, etc.). Device level design skills would be appreciated.

FUNDING AND PARTNERS

The post doctoral contract will be funded by the ANR (French National Research Agency) in the framework of the « SCREAM » ANR project selected in 2024. The work will be done in collaboration between LIRMM (UMR 5506 Université de Montpellier / CNRS), SPINTEC (UMR 8191 CEA / CNRS / Université Grenoble-Alpes / Grenoble INP) and EMSE (Ecole des Mines de Saint Etienne).

CONTACT

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